



TO : General

DATE : Jan. 25, 2013

SAMSUNG TFT-LCD

MODEL NO.: LTN156AT19-0

NOTE: Extension code [- 0xx]

→ LTN156AT19-0xx

Surface type [A/G]

Any modification of Spec is not allowed without SEC's permission

Application engineering part, Mobile Division Samsung Electronics Co., Ltd.

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REVISION HISTORY

Product Information

Date	Revision No.	Page	Summary
Jan, 25. 2013	A00	All	The approval specification of 15.6" SMS HD was issued first.

CODE REVISION HISTORY

Date	Model.	Revision No.	Summary
June, 15. 2011	LTN156AT19	001	Basic model

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GENERAL DESCRIPTION

DESCRIPTION

LTN156AT19 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices.

This model is composed of a TFT LCD panel, a driver circuit and a backlight unit.

The resolution of a 15.6" contains 1366 x 768 pixels and can display up to 262,144 colors.

6 O'clock direction is the optimum viewing angle.

FEATURES

- High contrast ratio
- HD(1366 x 768 pixels) resolution
- Fast Response
- LED Back Light with embedded LED Driver
- DE (Data enable) only mode
- 3.3V LVDS Interface
- Onboard EEDID chip

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	344.232 (H) x 193.536 (V) (15.6"diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1366 * 768	pixel	
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.252 (H) x 0.252 (V) (TYP.)	mm	
Display Mode	Normally white		
Surface treatment	Haze 25%, Hardness 2H		A/G

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Mechanical Information

	Item	Min.	Тур.	Max.	Unit	Note
	Horizontal (H)	358.8	359.3	359.8	mm	
Module size	Vertical (V)	209.0	209.5	210.0	mm	
Size	Depth (D)	-	-	4.0	mm	
	Weight	-	-	430	g	

Note (1) Measurement condition of outline dimension

. Equipment : Bernier Calipers . Push Force : 500g ·f (minimum)

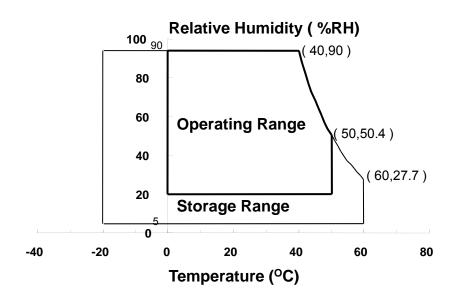
1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below. 95 % RH Max. $(40 \, ^{\circ}\text{C} \ge \text{Ta})$

Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation



- (2) 2ms, half sine wave, one time for $\pm X$, $\pm Y$, $\pm Z$.
- (3) 5 500 Hz, random vibration, 30min for X, Y, Z.
- (4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

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1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

 $V_{DD} = 3.3V$, $V_{SS} = GND = 0V$

ltem	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{DD}	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)
Logic Input Voltage	Vin	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)

Note (1) Within Ta (25 \pm 2 $^{\circ}C$)

(2) BACK-LIGHT UNIT

Ta = 25 ± 2 °C

Item	Symbol	Min.	Тур.	Max.	Unit	Note
LED Current	lL	-	22	-	mArm s	(1)
LED Voltage	VL	-	3.2	-	V	(1)

Note 1) Permanent damage to the device may occur if maximum values are exceeded Functional operation should be restricted to the conditions described under normal operating conditions.

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2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5). Measuring equipment: TOPCON SR-3

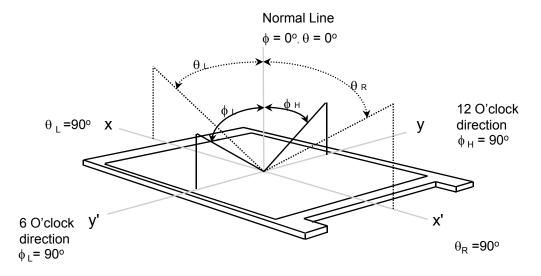
* Ta = 25 ± 2 °C, V_{DD}=3.3V, fv= 60Hz, f_{DCLK} = 70.7MHz, IF = 100% duty

Item		Symbol	Conditio n	Min.	Тур.	Max	Unit	Note									
Contrast I (5 Poil		CR		300	-	-	-	(1), (2), (5)									
Response Tir (Rising + F		T _{RT}		-	16	25	msec	(1), (3)									
Average Lur of White (5		YL,AVE	Normal	200	220	-	cd/m ²	IF=100% duty (1), (4)									
	Dod	Rx	Viewing		0.570												
	Red	Ry	Angle $\phi = 0$		0.340												
	0,,,,,,	Gx	θ = 0		0.330												
Color	Green	Gy		Тур-	0.560	Тур											
Chromaticity (CIE)	Dive	Вх		0.03	0.160	+0.03	-										
	Blue	Вү				0.135			-			(1), (5)					
	\	Wx			0.313												
	White	Wy			0.329												
	Hor.	θι		40	45	-											
Viewing	HOI.	θн	CR ≥ 10	40	45	-	Degrees										
Angle	Ver.	фн	At center	15	15	-											
		фL	30		30-	-											
Color Ga	mut	CG		-	45	-	%										
13 Poir White Var		δι		-	-	2.0	-	(6)									

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Note 1) Definition of Viewing Angle : Viewing angle range $(10 \le C/R)$

Product Information

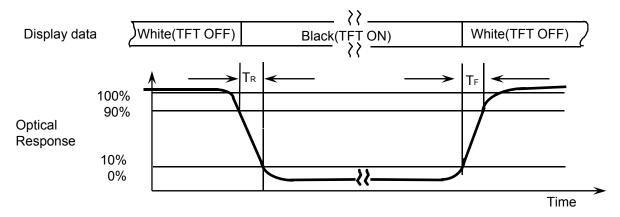


Note 2) Definition of Contrast Ratio (CR): Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points(4, 5, 7, 9, 10)

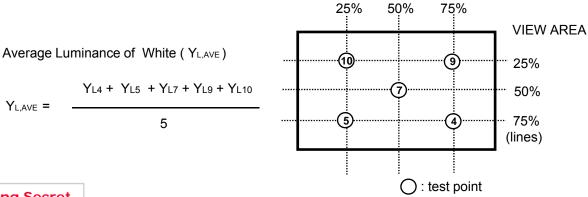
$$CR = \frac{CR(4) + CR(5) + CR(7) + CR(9) + CR(10)}{5}$$

Points : (4), (5), (7), (9), (10) at the figure of Note (6).

Note 3) Definition of Response time:



Note 4) Definition of Average Luminance of White: measure the luminance of white at 5 points.



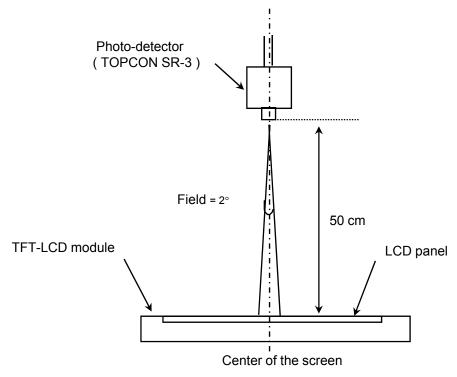
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Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room.

30 min after lighting the backlight. This should be measured in the center of screen.

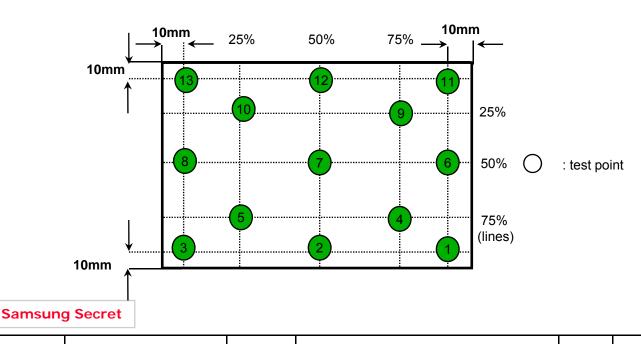
IF current: 22mA

Environment condition : Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

Note 6) Definition of 13 points white variation (δ L), CR variation (CVER) [1 ~ 13] δ L = $\frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$



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3. ELECTRICAL CHARACTERISTICS

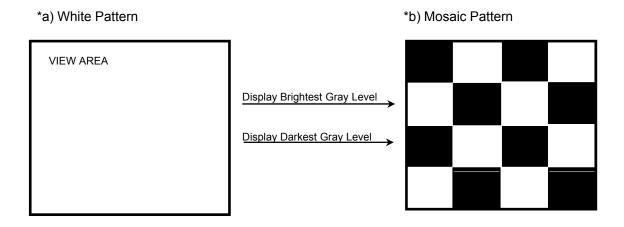
3.1 TFT LCD MODULE

Ta= 25 ± 2 °C

Item		Symbol	Min.	Тур.	Max.	Unit	Note
Voltage of Power	Supply	V _{DD}	3.0	3.3	3.6	V	
Differential Input	High	VIH	-	-	+100	mV	V _{CM} = +1.2V
Voltage for LVDS Receiver Threshold	Low	VIL	-100	-	-	mV	
Vsync Frequency		fv	-	60	-	Hz	
Main Frequency		fdclk	66.14	70.7	83.88	MHz	-
Rush Current		Irush	ı	-	1.5	Α	(4)
	White		-	230	-	mA	
Current of Power Supply	Mosaic	IDD	-	230	-	mA	*a),b),c)
	V.stripe		-	300	350	mA	

Note (1) Display data pins and timing signal pins should be connected.(GND = 0V)

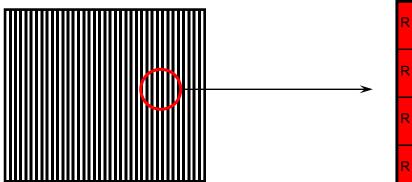
- (2) $f_V = 60$ Hz, $f_{DCLK} = 72.33$ MHZ, $V_{DD} = 3.3$ V, DC Current.
- (3) Power dissipation pattern

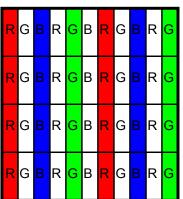


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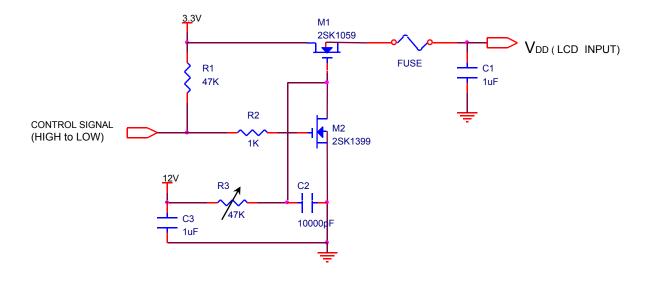


*c) 1dot Vertical stripe pattern

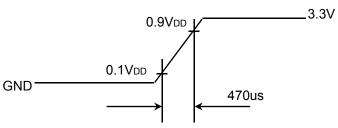




4) Rush current measurement condition



VDD rising time is 470us



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3.2 LED Driver

- On board LED Driver (Intersil)

Ta= 25 ± 2 °C

Item-	Symbol	Min.	Тур.	Max.	Unit	Note
Input Voltage	Vin	7	12	20	V	-
Input Current	I	-	270	-	mA	-
nower consumption	Р	ı	0.9	1.0	W	@ 60nit
power consumption	Г	-	3.3	3.5	W	@ Max
EN control lovel	ON	2.0	1	-	V	
EN control level	OFF	-	-	0.8	V	
DIA/M control lovel	ON	2.0	-	-	V	
PWM control level	OFF	-	-	0.8	V	
PWM Control Duty	D	5	-	100	%	PWM freq : 200Hz~10KHz
Ratio	U	10	-	100		PWM freq : 1KHz~10KHz
External PWM Dimming Control Frequency (BLIM)	F _{ВЫМ}	0.2	1	10	kHz	
Operating Life Time	Hr	10,000	-	-	Hour	

Note (1) Life time (Hr) of LEDs can be defined as the time in which it continues to operate under the condition Ta= 25 ± 2 °C and IF = 22mArms until one of the following event occurs. When the brightness becomes 50% or lower than the original.

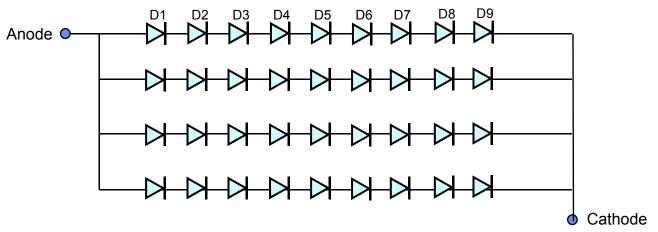
3.3 BACK-LIGHT UNIT

Ta= 25 \pm 2 °C

Item	Symbol	Min.	Тур.	Max.	Unit	Note
LED Forward Current	IF	-	22	-	mA	
LED Forward Voltage	VF	3.0	3.2	3.4	V	
LED Array Voltage	VP	-	36	-	V	
BL consumption	Р	-	-	3.3	W	@ MAX

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Product Information 4. BLOCK DIAGRAM 4.1 TFT LCD Module User LVDS LVDS Input/ m-LVDS Output m-LVDS Connector **Timing Controller** Source Driver 15.6" HD TFT-LCD **Panel** (1366*768)DC-DC Gamma Converter Generator LED DRIVER **VCOM** Generator LED FPC connector Gate Pulse Generator Gamma --> Data Signal PVDD -Control Signal **VCOM** AVDD Gate IC Signal Von/Voff → DVDD -**VBL** VLED & FB 4.2 LED placement structure



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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector: I-PEX 20455-#40E-## or equivalent)

No.	Symbol	Function	Polarity	Remarks
1	NC	No Connection (Reserved for supplier)		
2	AVDD	Power Supply 3.3V (typical)		
3	AVDD	Power Supply 3.3V (typical)		
4	DVDD	DDC 3.3V power		
5	NC	No Connection		
6	SCL	DDC Clock		
7	SDA	DDC data		
8	RIN0-	-LVDS differential data input (R0-R5, G0)	Negative	
9	RIN0+	+LVDS differential data input (R0-R5, G0)	Positive	
10	GND	Ground		
11	RIN1-	-LVDS differential data input (G1-G5, B0-B1)	Negative	
12	RIN1+	+LVDS differential data input (G1-G5, B0-B1)	Positive	
13	GND	Ground		
14	RIN2-	-LVDS differential data input (B2-B5, HS, VS, DE)	Negative	
15	RIN2+	+LVDS differential data input (B2-B5, HS, VS, DE)	Positive	
16	GND	Ground		
17	CLK-	-LVDS differential clock input	Negative	
18	CLK+	+LVDS differential clock input	Positive	
19	GND	Ground		
20	NC	No connection		
21	NC	No connection		
22	GND	Ground		
23	NC	No connection		
24	NC	No connection		
25	GND	Ground		
26	NC	No connection		
27	NC	No connection		
28	GND	Ground		
29	NC	No Connect		
30	NC	No Connect		

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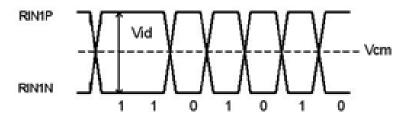
No.	Symbol	Function	Polarity	Remarks
31	VSSLED	Ground – LED		
32	VSSLED	Ground – LED		
33	VSSLED	Ground – LED		
34	NC	No Connect		
35	PWM	System PWM Signal Input (+3.3V Swing)		
36	LED_EN	LED enable pin (+3.3V Input)		
37	NC	No Connect		
38	VDDLED	LED power		
39	VDDLED	LED power	_	
40	VDDLED	LED power		

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5.2 LVDS Interface

5.2.1 LVDS DC Input

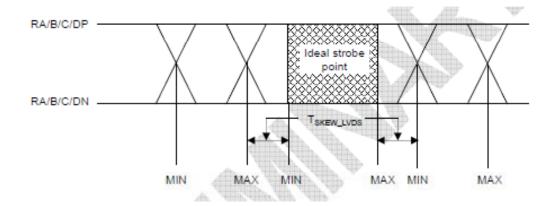
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
LVDS Differential Voltage	VID	200	_	600	mV	
Input Common Mode Voltage	V _{CM}	0.4	1.2	1.7	V	



5.2.1 LVDS AC Input

ITEM		SYMB0L	MIN.	TYP.	MAX.	UNIT	NOTE
LVDS input Clo	ock Frequency	F _{CLK_LVDS}	30		100	Mhz	
LVDS RX skew	100MHz		_	_	270	ps	(1),(2)
Right margin	50MHz	Т	_	_	700	ps	(1),(2)
LVDS RX skew	100MHz	T _{RSRM}	-270	-	_	ps	(1),(2)
Left margin	50MHz		-700	_	_	ps	(1),(2)
Maximum deviation of LVDS input clock during SSCG		F _{CLK_DEV}	_	_	± 3	%	(3)
Modulating frequency of LVDS input clock during SSCG		F _{CLK_MOD}	30	_	300	KHz	(3)

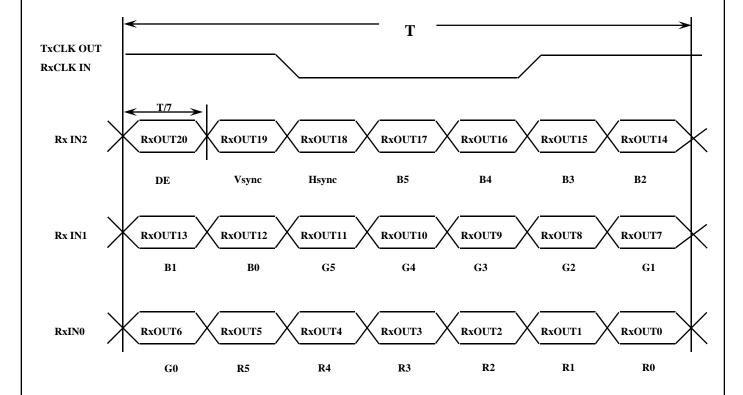
Note (1): LVDS Receiver Skew (Strobe) Margin



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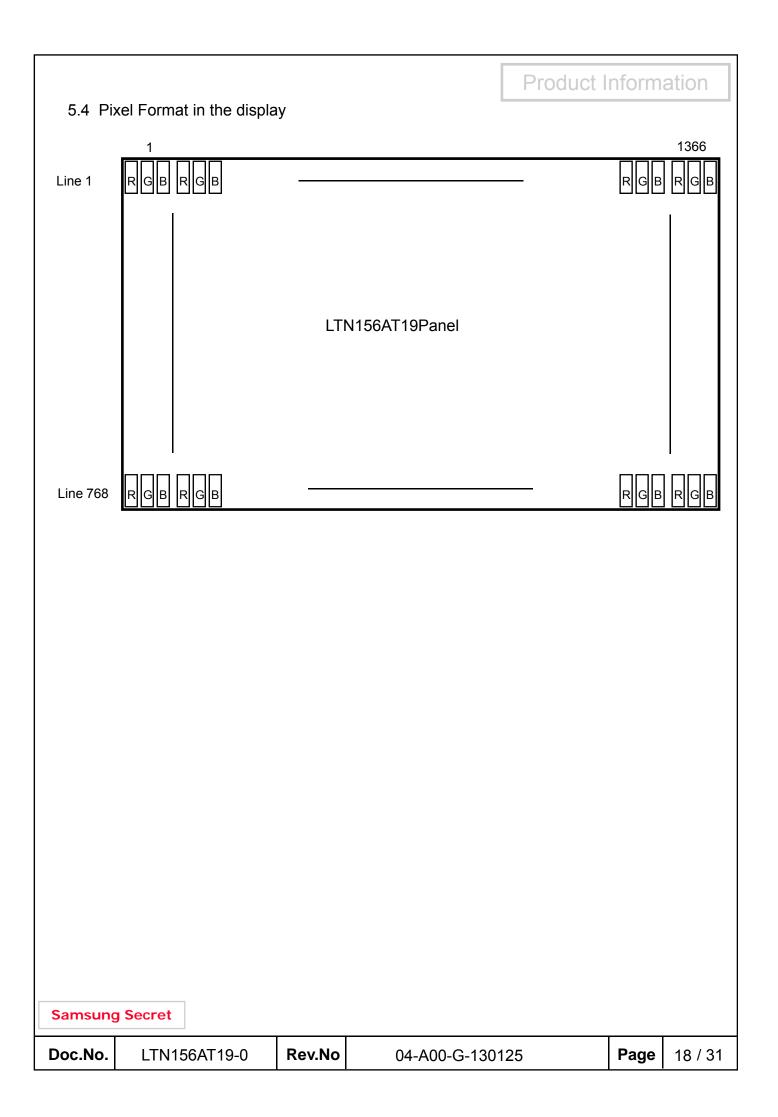
5.3 Timing Diagrams of LVDS For Transmission

LVDS Receiver : Integrated T-con



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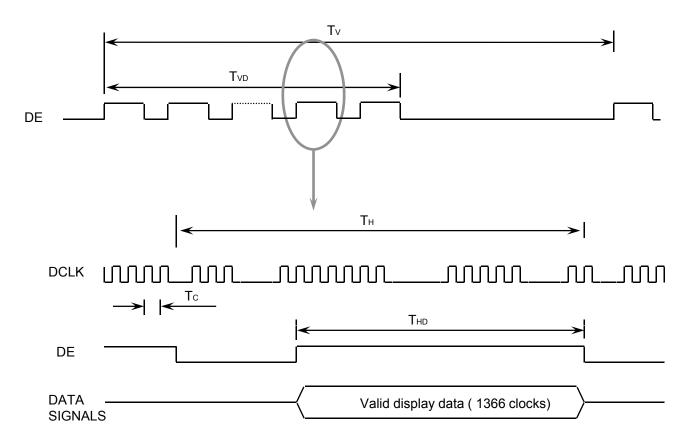


6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
Frame Frequency	Cycle	TV	773	790	810	Lines	
Vertical Active Display Term	Display Period	TVD	ı	768	-	Lines	
One Line Scanning Time	Cycle	TH	1426	1526	1726	Clocks	
Horizontal Active Display Term	Display Period	THD	-	1366	-	Clocks	

6.2 Timing diagrams of interface signal

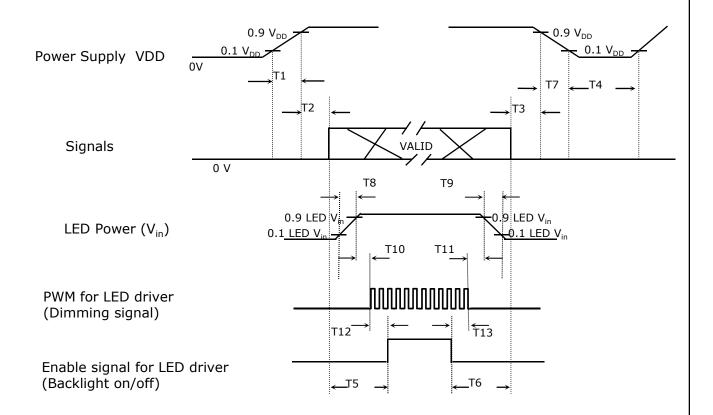


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6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Timing (ms)	Remarks		
0.5 <t1≤10< td=""><td colspan="2">V_{DD} rising time from 10% to 90%</td></t1≤10<>	V _{DD} rising time from 10% to 90%		
0 < T2 ≤50	Delay from V _{DD} to valid data at power ON		
0 < T3 ≤50	Delay from valid data OFF to ${ m V}_{ m DD}$ OFF at power Off		
500 ≤T4	V _{DD} OFF time for Windows restart		
300 ≤T5	Delay from valid data to B/L enable at power ON		
200 ≤T6	Delay from valid data off to B/L disable at power Off		
0 < T7 ≤10	V _{DD} falling time from 90% to 10%		
0.5 <t8≤10< td=""><td colspan="2">LED V_{in} rising time from 10% to 90%</td></t8≤10<>	LED V_{in} rising time from 10% to 90%		
0.5 <t9≤10< td=""><td colspan="2">LED V_{in} falling time from 90% to 10%</td></t9≤10<>	LED V _{in} falling time from 90% to 10%		
0 ≤T10	Delay from LED driver Vin rising time 90% to PWM ON		
0≤T11	Delay from PWM Off to LED driver Vin falling time 10%, Must Keep rule		
0≤T12	Delay from PWM ON to B/L Enable ON, Must Keep rule		
0 ≤T13	Delay from B/L Enable Off to PWM Off		

Power Sequence & Timing Parameters

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6.3 Power ON/OFF Sequence

NOTE.

- (1) The supply voltage of the external system for the module input should be the same as the definition of VDD.
- (2) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become white.
- (3) In case of VDD = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.